The Spiral2 LLRF FPGA design applied to the control of the RFQ

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Abstract

CEA/Saclay developed the LLRF system to control the accelerator cavities of Spiral2. Its architecture, based on in-house VME64x boards equipped with a Virtex-5 FPGA, was described in the previous LLRF workshops [1] [2].

The FPGA VHDL/C developments follow a modular approach to build a **generic design** applicable to all the cavity types (RFQ, normal conducting rebunchers and superconducting resonators).

The poster presents an overview of the hardware and software design, split into a softcore processor and VHDL modules.

The emphasis is put on the **RFQ control** which is the most complex case: this cavity is fed with four power amplifiers and cannot be driven at fixed frequency during startup.

The FPGA design has been enhanced with **a perturbation generator** and **a frequency shifter** which are useful for the evaluations of the regulation performances, the tuning check and the automatic tracking of the resonance frequency during the RFQ startup.

LLRF / RFQ architecture description

The RFQ is the only cavity supplied with 4 power amplifiers, thus 4 RCAV are needed. The 4 incident voltages from the amplifiers must be kept in constant phasis and equal relations. To do so, one master RCAV regulates the cavity field and 3 slaves modules regulate the incident wave Uci of their own amplifiers. The master incident wave is used as a set points for the 3 slaves feedback loops (see Figure 2).

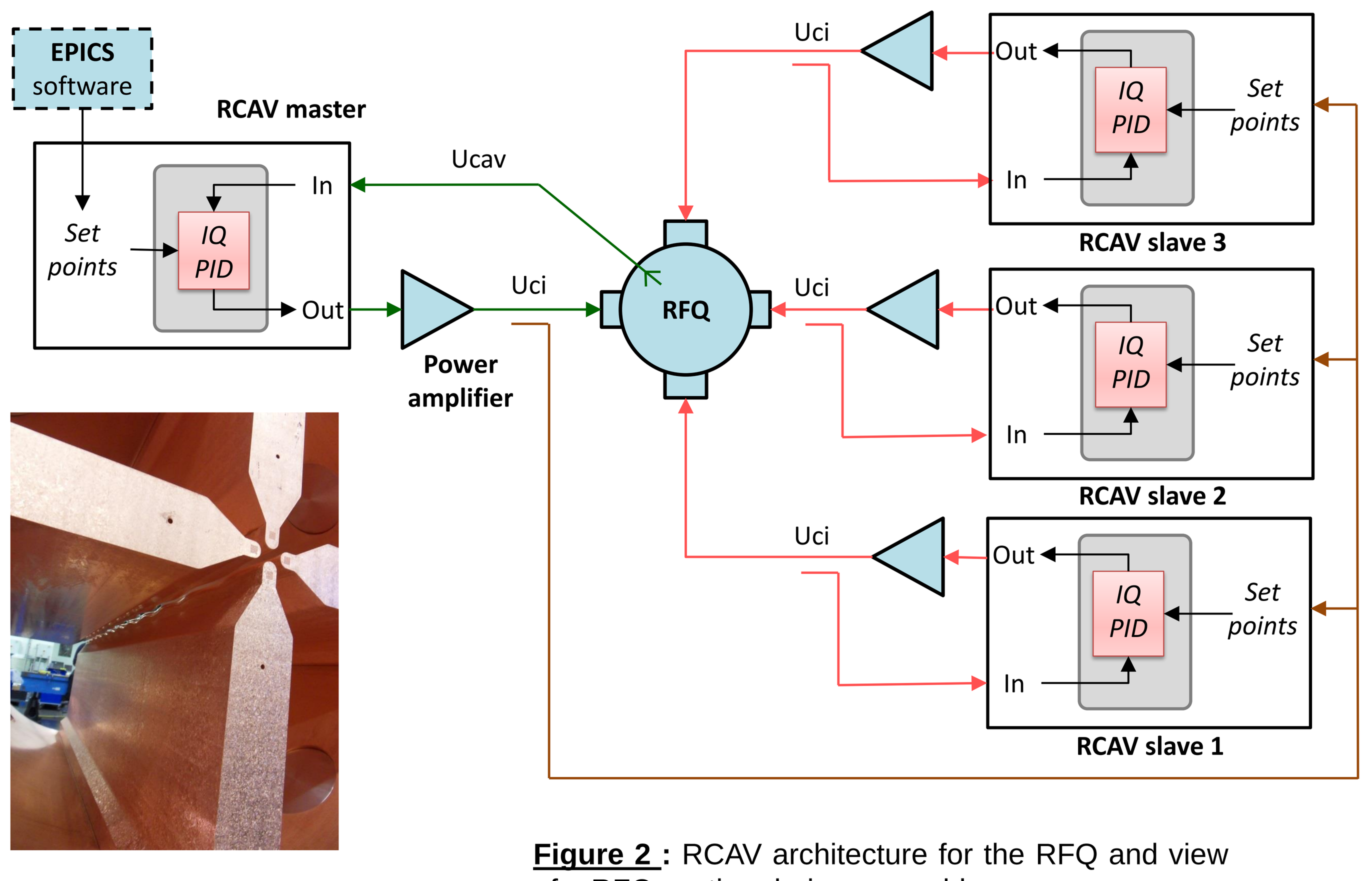


Figure 2 : RCAV architecture for the RFQ and view of a RFQ section during assembly.

The figure 3 shows the step response (to a set point change) of the master and slave feedback loops. The latency time of a slave feedback loop is about 1.14 µs.

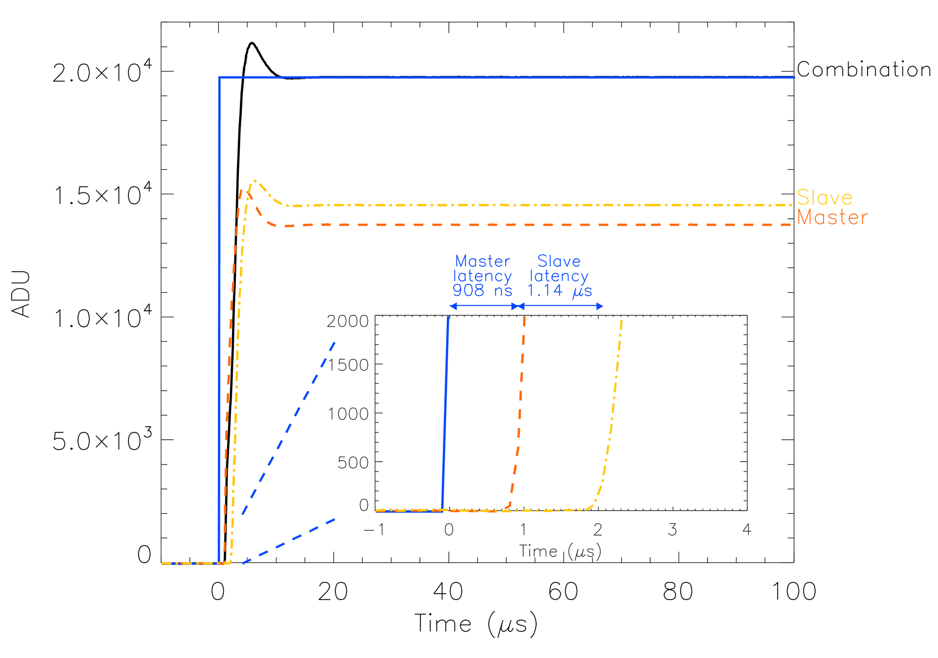


Figure 3 : Master and one slave amplitude transient response.

Perturbation generator for the regulation evaluation

In order to evaluate the regulation performances, we use a sinus wave generator which acts like a perturbation source. The amplitude and the frequency are defined in the HMI under EPICS. The CORDIC performs the polar to rectangular conversion. (see figure 4).

The figures 5 and 6 show spectra of the cavity field. A rejection exceeding 40 dB at 1 KHz is measured.

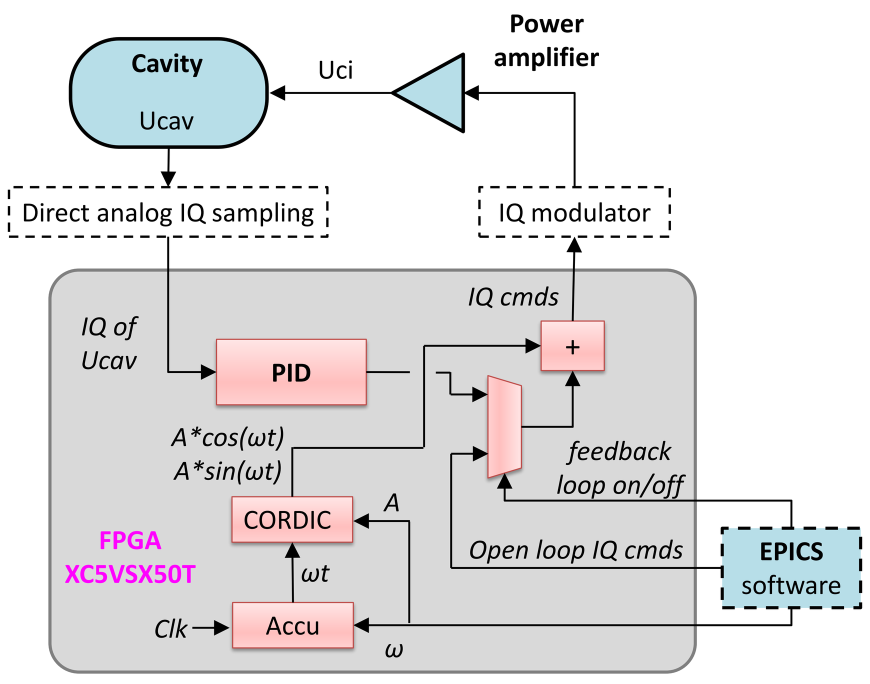


Figure 4 : View of the perturbation generator with the IQ control loop.

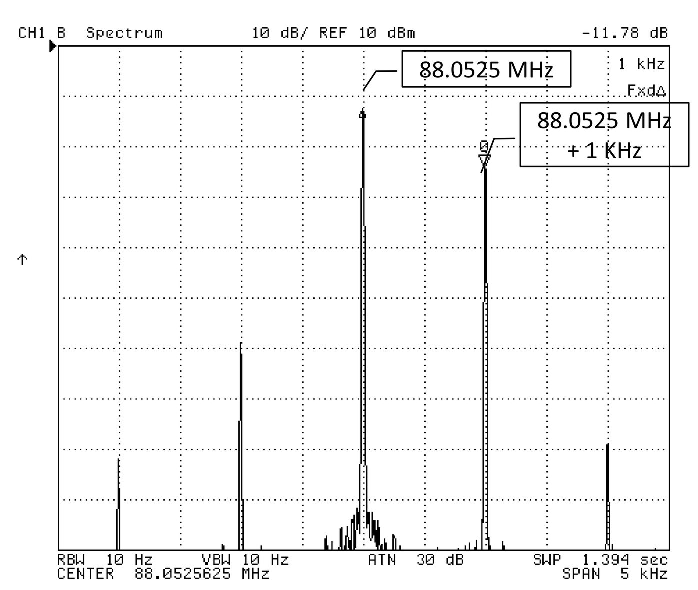


Figure 5 : Accelerator reference frequency (88.0525 MHz) and 1 kHz perturbation signal. The IQ control loop is open.

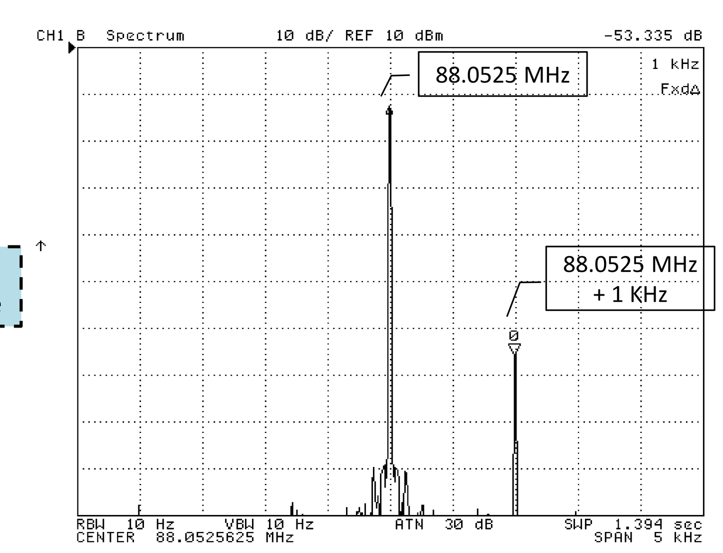


Figure 6 : Accelerator reference frequency (88.0525 MHz) and 1 kHz perturbation signal. The IQ control loop is closed.

Generic hardware/software description

For each cavity, the main LLRF functionalities are grouped in a set of two boards named RCAV excepted for the RFQ. A RCAV consists of two VME64X electronic boards :

- One main digital board built around a powerful Virtex-5 - XC5VSX50T (Xilinx) FPGA to perform digitally the LLRF operations.
- One rear I/O analog board for the analog processing of the RF signals (like analog ↔ digital conversions or I,Q modulation) and the low frequency signals.

The FPGA design is divided in two main parts :

- A RF part including fast digital processing (DSP functions)
- A slow processing part (softcore processor)

Each RCAV works with the VME CPU for the upper level EPICS Control/Command.

The generic hardware and software embedded in the FPGA are used for all cavities (RFQ, superconducting cavities, etc.). The cavity type is a parameter of the FPGA design.

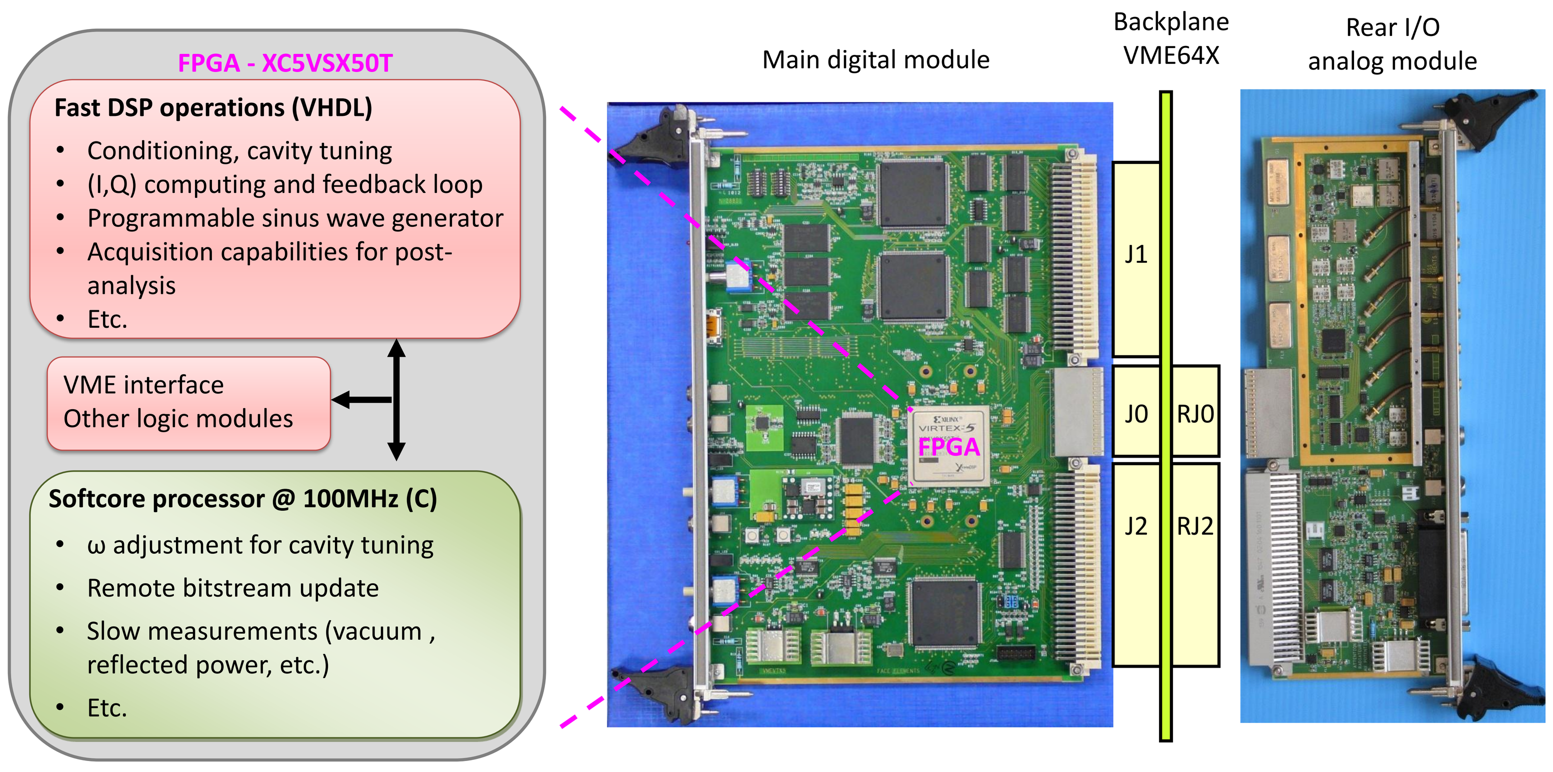


Figure 1 : RCAV boards and FPGA functionalities overview.

Frequency shifter and cavity tuning

The frequency shifter is a FPGA generic functionality. It can be used for the RFQ startup and with all cavities to check the tuning.

The RFQ tuning system, based on the temperature control of five tons of copper, is very slow; during startup the RFQ is rapidly detuned because of the increasing dissipated power.
To allow setting the RFQ RF in a reasonable amount of time, a frequency generator is used to find and follow the resonance frequency.

We first thought using an external synthesizer to implement this function. This choice would have led to an injector rack different from the others. For the sake of simplicity and hardware uniformity, we built a frequency shifter in the FPGA (see Figure 7).

The frequency shift is applied to the Uci set points control loop to minimize spurious frequencies due to the analog IQ modulator. (See Figure 8).

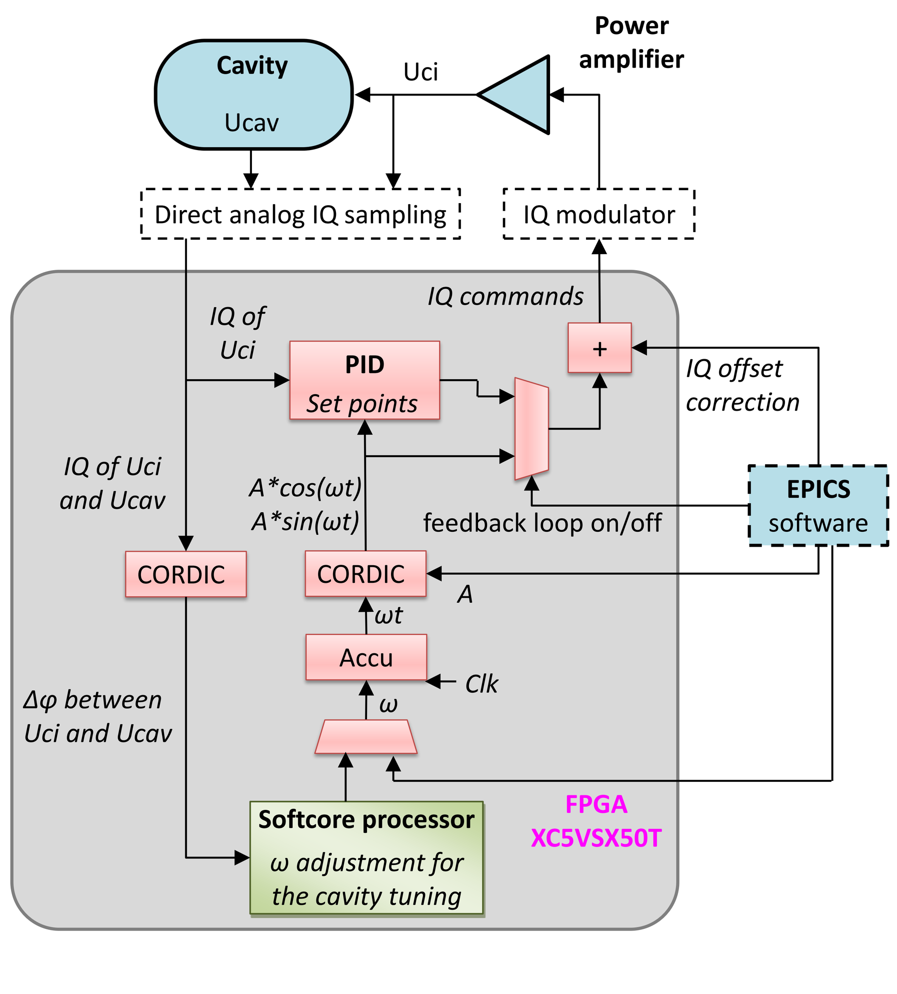
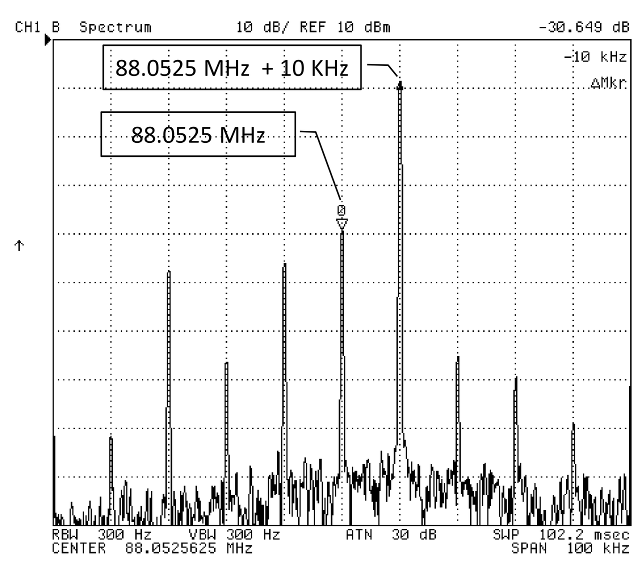
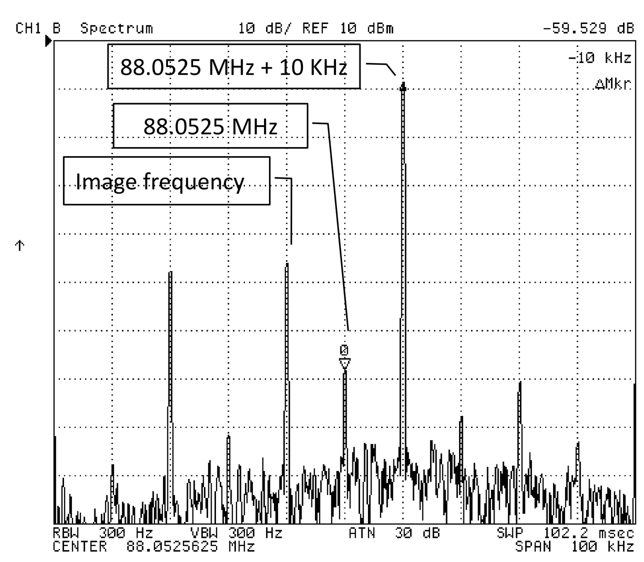


Figure 7 : Automatic adjustment (using a frequency shifter) of the power amplifier frequency of one cavity to match the resonance frequency.

I/Q analog offset are not corrected. Feedback loop is OFF.



I/Q analog offset are corrected after calibration. Feedback loop is OFF
The image frequency is not lowered



Feedback loop is ON
The rejection of image and parasitic frequencies is better without calibration need

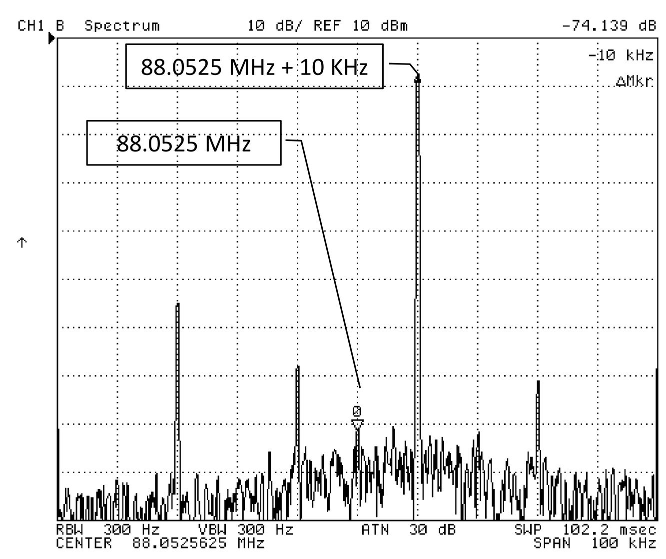


Figure 8 : Experimental results for a 10 KHz shift from 88.0525 MHz.

Conclusion

The development work presented in this poster allows a uniform LLRF hardware for the Spiral2 accelerator, as well as a unique FPGA design for all the cavity types.

The RFQ architecture has been tested successfully with 2 RCAV.

The next step is the test with the actual RFQ that will start before the end of 2013.

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References

[1] P. De Antoni, P. Galdemard. The architecture of the low level RF electronics for SPIRAL 2, *Low Level Frequency Workshop, October 2007, Knoxville, TN, USA*
[2] Y. Mariette, S. Sube. FPGA architecture for the Spiral2 digital low level RF, *Low Level Radio Frequency Workshop, October 2011, Hamburg, Germany*